MICROPROCESSOR COMPRISING AN INSTRUCTION FOR INVERTING BITS IN A BINARY WORD

Abstract of the Disclosure

A microprocessor comprises a central processing unit having an arithmetic and logic unit with two inputs and one input fed-back to one of the inputs through a data path. The arithmetic and logic unit performs arithmetic and logic operations on binary words temporarily stored within registers in the central processing unit. The central processing unit further includes a shift unit in the data path of the arithmetic and logic unit for performing operations to shift bits in the binary words applied thereto. A selection circuit selects a shift operation to be performed. An inverting circuit inverts the ordering of the bits in the binary words applied thereto, which are in the data path of the arithmetic and logic unit, and a selection circuit selects the inversion operation when the latter is required.